

6

09/932,704 Byers 41-3

Remarks

Reconsideration of the application and allowance of all claims pending are respectfully requested. No amendments to the claims are requested to be entered in view of the Office Action having been made final. Claims 1-3 and 5-18 are pending.

Claim Rejection - 35 U.S.C. §103:

Claims 1-5, 5-9, and 11-18 are rejected under 35 U.S.C. §103 as being unpatentable in view of Corfield (U.S. Patent No. 4,682,323) and Hale (U.S. Patent No. 5,572,349). This rejection is respectfully traversed.

MPEP §706.02(j) states: "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." (Emphasis added.)

For explanatory purposes, applicants discuss herein one or more differences between the applied reference and the claimed invention with reference to one or more parts of the applied reference. This discussion, however, is in no way meant to acquiesce in any characterization that one or more parts of the applied reference correspond to the claimed invention.

Claim 1 is directed to a method for use in a stored program controlled system with a plurality of processing units and a signal generator that interconnects the processing units using time division multiplexing over a free space optical beam line. A common clock signal is generated at a signal generator and distributed over the free space optical beam line to the processing units. A common synchronization signal is generated at the signal generator based on the clock signal and

distributed over the free space optical beam line to the processing units. A time slot counter at each processing unit is synchronized to the clock signal and a common synchronization signal. A message pattern containing a processing unit's address and corresponding time slot map data is generated at the signal generator and distributed over the free space optical beam line to the processing units. Maintained at each processing unit is a time slot map based on the received time slot map data associated with the address of the processing unit. An enable signal is derived from the contents of the time slot map to enable transmission of data onto the beam line. Another enable signal is derived from the contents on the time slot map to enable one or more receivers to extract data from the beam line.

In the Office Action the step in claim 1 of generating at the signal generator a common clock signal was said to be taught by Corfield as the "master clock" of column 2, lines 60-66. The further requirement of distributing a common clock signal over the free-space optical beam line to all processing units was said to be taught by Corfield at column 2, lines 33-34. The cited sections of Corfield do not provide teachings of the required claim limitations for the following reasons.

Corfield is directed to providing light beam signal paths between integrated circuits. Although a guided light transmission system is illustrated, it is mentioned in Corfield at column 2, lines 33-34, that in some applications the guided transmission system could be replaced by a free space transmission between the adjacent circuits. In accordance with the first generating step of claim 1, a signal generator generates a common clock signal and distributes it over the free space optical beam line to all processing units. This requirement has two parts: (a) the generation of a common clock signal; (b) the transmission of the common clock signal over the free space optical beam line to all processing units. It is stated in Corfield that a clock generator on each chip runs at the commutation rate and that this is typically provided by master clock on one chip controlling slave generators on the other chips; column 2, lines 60-66. However, there is no teaching in Corfield that the master clock is transmitted as a signal over the optical beam. Further, there is nothing about the explicit teachings of Corfield that would make it implicit or inherent that a master clock signal would have been transmitted over the optical beam. The general representations of the integrated circuit devices 11 and 12 in Corfield do not show or

explain how many of the required functions would be performed or of other connections. For example, no means is shown for supplying DC power to the integrated circuit devices or other connections or interactions with other devices. Signal paths and connections other than the optical beam would typically exist between the integrated circuit boards of Corfield. One of ordinary skill in the art based on the teachings of Corfield would understand this and would not find it inherent that a common clock signal was or would have to be distributed over the optical beam line. In order for a teaching to be found inherently present in a reference, one of ordinary skill in the art would have to understand that the unstated teaching would have to have been practiced to accomplish actions/structure of the embodiment of the reference. As explained above, it is not inherent that a common clock signal was distributed over an optical beam line based on the disclosed embodiment in Corfield. Hence, Corfield cannot support this alleged teaching. Since the other applied reference, Hale, is not relied upon with regard to this teaching, none of the applied references provide the required teaching and hence the rejection of claim 1 should be withdrawn.

Claim 1 further requires generating a common synchronization signal based on the clock signal and distributing the common synchronization signal over the free space optical beam line to all processing units. In the Office Action this is alleged to correspond to the "common output signal" of column 2, lines 3-11, of Corfield. This cited text portion reads:

"Each pad 14, 14a is coupled by electronic switch 16, 16a, controlled by a clock generator 23, 23a, to the signal outputs 21, 21a whereby signals generated at those outputs may be time division multiplexed to form a common output signal. This common output signal is superimposed or modulated on to an optical signal by the diode 15, 15a which optical signal is then coupled to the data highway 13, 13a by an input port 17, 17a."

The above text is referring to the time division multiplexing of signals from digital circuit 22 into a single stream of data to be transmitted as a serial output signal using a single optical diode 15. It should be noted that the time division multiplexing of the signals from the digital circuit 22 occurs on the circuit board using conventional wired paths that connects the digital circuit outputs to the optical diode. The "common output signal" referenced in the Office Action merely refers to the time division multiplexed stream of data from the digital circuit prior to being fed to

the optical diode for transmission. Such an action (nor the act of merely transmitting it by the optical diode) does not constitute nor is it equivalent to the distributing of a common synchronization signal over the free space optical beam line. One of ordinary skill in the art would not understand the mere transmission of a time multiplexed stream of data itself constituting the transmission of a common synchronization signal. There appears to be nothing in Corfield to suggest the transmission of an optical synchronization signal. Further, there is nothing inherent about the transmission of a time multiplexed data series itself that equates with the transmission of a synchronization signal. Hence, Corfield does not provide a teaching of this limitation and it is not inherent that the transmission of the time multiplexed that a series of Corfield constitutes an optical synchronization signal. The Hale reference was not relied upon regard to this limitation. Therefore, it is requested that the rejection of claim 1 under 35 U.S.C. 103 be withdrawn since none of the applied references, considered individually or in combination, supply the required limitation.

Claim 1 requires generating at the signal generator a message pattern containing a processing unit address and corresponding time slot map data, and distributing this message pattern over the free space optical beam line to all processing units. In the Office Action the time slot map data generation was indicated to be inherent in the "common output signal" and "master clock" of Corfield. The distributing of the time slot map data over the free space optical beam line to all processing units was alleged to be taught by Corfield at column 1, lines 26-33 and column 2, lines 12-22. The first text citation describes that the inputs of each circuit are controlled by clock so that each input is enabled only for a respective time slot of a received multiplexed signal. This teaching basically describes the demultiplexing of a multiplexed signal, but does not teach or suggest that a time slot map data itself was transmitted as an optical message. Further, it is not inherent that a time slot map would have ever had to have been transmitted as an optical signal. For example, each of the circuit boards could contain stored time slot definitions in nonvolatile memory that would define appropriate time slots to be used by each board for the transmission of data. Such time slot definitions would have been loaded into memory, e.g. an EEPROM, at the time of manufacture of the circuit board. Thus, it is not implicit or inherent at the time slot map would have had to been transmitted as optical signal. The second text citation merely describes that the photodetectors are controlled by a circuit clock so that each is enabled

10

09/932,704 Byers 41-3

only during its respective time slot. However, as explained above, this does not teach or suggest that a time slot map would have ever had to have been transmitted optically to the circuit boards. Therefore, Corfield does not provide a teaching of this requirement of claim 1, and the rejection of claim 1 on this ground should be withdrawn.

Claims that depend on claim 1 provide additional limitations of patentable significance when considered as a whole in combination with the parent claim.

Independent apparatus claim 12 was also rejected under 35 U.S.C. 103 for the same reasons applied to claim 1. Claim 12 is believed to be allowable for similar reasons as explained above with regard to claim 1.

Claims that depend on claim 12 provide further additional limitations that are believed to provide additional patentable significance when considered as a whole with claim 12.

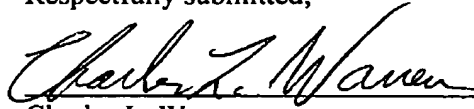
The Examiner rejected claim 10 under 35 U.S.C. 103 as being obvious further in view of Zikan (U.S. Patent 6,310,881). The Zikan reference was cited merely to supply a teaching relating to dynamic data flow control. It will be apparent that the combination of this reference with Hale and Corfield does not render the subject matter of claim 10 obvious since Corfield and Hale fail to provide the necessary teachings as discussed above. Therefore, the rejection of claim 10 should be withdrawn.

11

09/932,704 Byers 41-3

In view of the above amendments and remarks, allowance of all claims pending is respectfully requested. If a telephone conference would be of assistance in advancing the prosecution of this application, the Examiner is invited to call applicants' attorney.

Respectfully submitted,

A handwritten signature in cursive script, appearing to read "Charles L. Warren", written over a horizontal line.

Charles L. Warren
Attorney for Applicants
Reg. No. 27,407

Dated: September 24, 2005

PATTI & BRILL, LLC
Customer Number 47382